POLISHING PAD AND METHOD OF POLISHING WAFER

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a polishing pad and a method of polishing a wafer. More particularly, the present invention relates to a polishing pad and a wafer polishing method that can improve polishing efficiency.

Description of Related Art

[0002] In the fabrication of semiconductor devices, one way of increasing the level of integration in a memory wafer or a logic wafer is to increase the aspect ratio and the number of conductive circuit layers in a stack. However, as the number of stacked circuit layers in a multi-layered structure increases, undulation or warping of the surface of a chip frequently occurs. To remove such non-planarity from a wafer surface, special global planarization techniques are developed. When the special planarization technique is incorporated to the fabrication of semiconductor, a multi-layered stack with many conductive line layers can be produced with a relatively high yield. One of the earliest corporations using the global planarization techniques was IBM. The original method included performing a chemical-mechanical polishing (CMP) operation to form buried conductive lines in a damascene process. During the chemical-polishing operation, surface planarization is achieved through slurry of abrasive particles and relative motion between the surface of a wafer and a polishing pad with suitable elasticity and hardness.

[0003] However, dishing may occur when slurry with suspended abrasive particles is used in a chemical-mechanical polishing operation to remove dielectric material (for example, silicon oxide) on silicon nitride within the active region of a shallow trench isolation (STI) structure. Recently, a new type of chemical-mechanical polishing method requiring no slurry has been developed. The new polishing method is called 'fixed abrasive chemical-mechanical polishing (FA-CMP)'. In the FA-CMP technique, the abrasive particles are fixed onto a superficial layer of a polishing pad. In other words, the polishing pad has a sand-paper-like surface that directly functions as a polisher. One major advantage of this method is a relatively high polishing selectivity between the dielectric material (for example, silicon oxide) and the silicon nitride. Furthermore, the method has high planarization efficiency but causes very little dishing in the silicon oxide within a shallow trench isolation (STI) structure.

[0004] Figs. 1A to 1C are schematic cross-sectional views showing the steps in a conventional method for polishing a wafer. First, as shown in Fig. 1A, a polishing station 100 is provided. The polishing station 100 comprises a wafer holder 102, a polishing pad 104 and a polishing platform 106. The polishing pad 104 is located above the polishing platform 106. The polishing pad 104 includes a layer of adhesive compound 110 with suspended abrasive particles 108 therein and an array of fixed abrasive units 111 shaped like a triangular cone, a hexagonal cone or a circular cylinder. The wafer holder 102 grips a patterned wafer 114 with a silicon oxide layer 112 (for example, the silicon oxide material that fills the grooves of a STI structure) thereon.

[0005] As shown in Fig. 1B, a polishing operation is performed to remove a portion of the silicon oxide layer 112 above the wafer 114 so that the silicon oxide layer 112 is globally planarized. Since the silicon oxide layer 112 originally on the surface

of the wafer 114 is non-planar, the adhesive compound 110 of the polishing pad 104 is readily removed to expose various interior polishing particles 108 for polishing the wafer.

[0006] Thereafter, as shown in Fig. 1C, the polishing operation is continued until the silicon oxide layer 112 on the wafer 114 is completely planarized. However, as the silicon oxide layer 112 is gradually planarized, surface roughness of the silicon oxide layer 112 is reduced. In other words, the efficiency of removing the adhesive compound 110 within the polishing pad 104 diminishes. After performing the chemical-mechanical polishing operation for a while, roughness level of the silicon oxide layer 112 may be inefficient to remove the adhesive compound 110 for exposing the abrasive particles 108. That means, the polishing action weakens gradually. Hence, it may take a long time to complete a global planarization operation or else some residual silicon oxide may still be able to adhere to the active region at the end of a polishing operation.

[0007] Accordingly, the aforementioned fixed abrasive CMP technique has a low polishing rate and a reduced polishing efficiency when the surface to be polished is too smooth. Thus, the minimum thickness of a polished layer is often set to about 1000Å. Yet, the width of a STI gap-fill process is severely limited when the feature line width is only about 90nm or smaller. In other words, the fixed abrasive CMP technique will encounter severe restrictions if it is applied to produce the next generation of smaller size semiconductors. To be useful, the fixed abrasive chemical-mechanical technique must be improved so that a high polishing selectivity ratio can be maintained without causing dishing at the end of a polishing operation.

SUMMARY OF THE INVENTION

[0008] Accordingly, one object of the present invention is to provide a polishing pad capable of increasing the polishing rate of fixed abrasive chemical-mechanical polishing operation.

[0009] Another object of this invention is to provide a method for polishing a wafer capable of lifting the thickness restriction of the polished layer in the conventional method.

[0010] Still another object of this invention is to provide a method for polishing a wafer capable of increasing the width in a shallow trench isolation (STI) gap-fill process.

[0011] Still another object of this invention is to provide a method for polishing a wafer capable of roughening up the abrasive particles on a polishing pad in-situ while a wafer polishing operation is performed.

[0012] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a polishing pad. The polishing pad has a plurality of abrasive units thereon. Each abrasive unit comprises a layer of adhesive compound and a plurality of abrasive particles such as cerium oxide (CeO_2) evenly distributed within the adhesive layer. In addition, the surface of the abrasive unit in contact with the wafer is roughened.

[0013] This invention also provides a wafer polishing method. First, a first polishing pad is provided. The first polishing pad has a plurality of abrasive units each comprising a layer of adhesive compound having evenly distributed abrasive particles therein. The abrasive particles inside the adhesive layer are fabricated using cerium oxide (CeO_2), for example. Thereafter, a first polishing operation is carried out to

planarize the surface of a wafer above the first polishing pad. Next, a second polishing pad is provided. Similarly, the second polishing pad has a plurality of abrasive units each comprising a layer of adhesive compound having evenly distributed abrasive particles therein. The upper surface of each abrasive unit has a roughened surface and the abrasive particles inside the adhesive layer is fabricated using cerium oxide (CeO_2), for example. Finally, a second polishing operation is carried out above the second polishing pad.

[0014] This invention also provides an alternative wafer polishing method. First, a wafer holder suitable for grasping a wafer is provided. The wafer holder has a retainer ring. The retainer ring has a grooves patterned into various shapes including crosses, concentric rings, spiral patterns or a combination of the aforementioned. Thereafter, a polishing pad is provided. The polishing pad has a plurality of abrasive units each comprising a layer of adhesive compound with evenly distributed abrasive particles therein. With the wafer gripped firmly by the wafer holder, the wafer holder is pressed onto the polishing pad to carry out a polishing operation. During the polishing operation, the groove patterns on the retainer ring is in contact with the surface of the abrasive units. Through the groove patterns, the surface of contact between the abrasive units and the wafer is roughened.

[0015] Accordingly, this invention utilizes the roughened surface of a polishing pad (the polishing units) to perform a fixed abrasive chemical-mechanical polishing of a wafer. This resolves the issue of having a decreasing polishing efficiency resulting from a gradual lowering of surface roughness in a polish layer. Hence, the time for completing a global planarization is reduced and the possibility of having residual material on the surface is minimized.

[0016] Furthermore, because this invention uses the roughened surface of a polishing pad (the polishing units) to carry out a fixed abrasive chemical-mechanical polishing operation, thickness of the polishing layer no longer constitutes a restriction. This invention also removes the width restriction in a shallow trench isolation (STI) gap-fill process.

[0017] In addition, this invention also utilizes a wafer holder with a retainer ring having a groove pattern to execute a fixed abrasive chemical-mechanical wafer polishing operation. Through the groove pattern on the retainer ring, the polishing pad (the polishing units) is re-conditioned in-situ to maintain a rough surface. Therefore, the upper surface of the polishing pad is able to maintain a roughened surface despite the gradual reduction in the roughness level of the polished wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0019] Figs. 1A through 1C are schematic cross-sectional views showing the steps in a conventional method for polishing a wafer.

[0020] Figs. 2A through 2D are schematic cross-sectional views showing the steps for polishing a wafer according to one preferred embodiment of this invention.

[0021] Fig. 3 is a graph showing the effects various types of fixed abrasive units have on silicon oxide/silicon nitride polishing rate.

[0022] Figs. 4A and 4B are schematic cross-sectional views showing the steps in an alternative method of polishing a wafer.

[0023] Figs. 5A through 5C are top views of the retainer ring with various types of groove patterns as shown in Fig. 4A.

[0024] Fig. 6 is a graph showing the effects various types of retainer ring grooves have on silicon oxide/silicon nitride polishing rate.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0026] In this invention, silicon oxide is used as the dielectric material in the following illustration. However, the fixed abrasive chemical-mechanical polishing method can be applied to other types of material as well.

[0027] Figs. 2A through 2D are schematic cross-sectional views showing the steps for polishing a wafer according to one preferred embodiment of this invention. As shown in Fig. 2A, a polishing station 200 is provided. The polishing station 200 includes a wafer holder 202, a first polishing pad 204 and a polishing platform 206. The first polishing pad 204 is located above the polishing platform 206. Furthermore, the first polishing pad 204 comprises a plurality of abrasive units 211. The abrasive units 211 are shaped into a triangular cone, hexagonal cone or circular cylinder and set up as an array. Each abrasive unit 211 comprises a layer of adhesive compound 210 with a plurality of evenly distributed abrasive particles 208 therein. The adhesive

compound 210 is an adhesive resin, for example. Aside from the abrasive units 211, the first polishing pad 204 also has a sub-pad (not shown) and a polishing platen (not shown) underneath. The platen is fabricated from a material including, aluminum alloy or stainless steel and the sub-pad is fabricated from a material including plastic, rubber or acrylic, for example. In addition, the wafer holder 202 grips a wafer 214 with a patterned silicon oxide layer 212 thereon. Note that if the layer to be polished is a silicon oxide, cerium oxide (CeO_2) abrasive particles 208 are preferably used because it has a higher polishing selectivity relative to the silicon oxide.

[0028] As shown in Fig. 2B, a first polishing step is carried out on the surface of the first polishing pad 204 so that the silicon oxide layer 212 on the wafer 214 is planarized. Since the silicon oxide layer 212 has an uneven surface initially, a portion of the adhesive compound 210 constituting the abrasive units 211 can be removed to expose the abrasive particles 208 (for example, cerium oxide CeO_2). The exposed abrasive particles 208 has the capacity to grind down the silicon oxide layer 212 on the wafer 214 and repeats the following reactivation continuously: (1) the rough silicon oxide layer 212 scratches away a portion of the adhesive compound 210 and exposes the abrasive particles 208; (2) the abrasive particles 208 grind down the silicon oxide layer 212 and blunt itself at the same time; and (3) the uneven silicon oxide layer 212 continues to remove some adhesive compound 210 to expose fresh abrasive particles 208 until the silicon oxide layer 212 is completely planarized.

[0029] However, as the silicon oxide layer 212 is gradually planarized, roughness on the surface of the silicon oxide layer 212 is also reduced. Since the capacity to remove adhesive compound 210 from the polishing pad 204 will drop after a

while, the polishing rate will drop. Therefore, in the following, another polishing step is carried out using a second polishing pad with a roughened surface.

[0030] As shown in Fig. 2C, another polishing station 300 with major elements identical to the previous one is provided. The second polishing pad 216 has a roughened surface. The second polishing pad 216 comprises a plurality of abrasive units 217. The abrasive units 217 are shaped into a triangular cone, hexagonal cone or circular cylinder and set up as an array. Each abrasive unit 217 comprises a layer of adhesive compound 210 with a plurality of evenly distributed abrasive particles 208 therein. The roughened surface of the second polishing pad 216 has a conical or a cylindrical shape, for example. Note that if the layer to be polished is silicon oxide, cerium oxide (CeO_2) abrasive particles 208 are preferably used because it has a higher polishing selectivity relative to the silicon oxide. In addition, the second polishing pad 216 also has a sub-pad (not shown) and a polishing platen (not shown) underneath. The platen is fabricated from a material including, aluminum alloy or stainless steel and the sub-pad is fabricated from a material including plastic, rubber or acrylic, for example.

[0031] As shown in Fig. 2D, a second polishing operation is carried out on the second polishing pad 216 so that the silicon oxide layer 212 on the wafer 214 is planarized. Although the surface of the silicon oxide layer 212 is nearly planar and can hardly remove the adhesive compound 210 to expose the abrasive particles 208, the roughened abrasive units 217 on the second polishing pad 216 provides polishing capability. Therefore, the polishing rate can be maintained despite a gradual drop in surface roughness of the polished layer (for example, the silicon oxide layer 212).

[0032] Fig. 3 is a graph showing the effects various types of fixed abrasive units have on silicon oxide/silicon nitride polishing rate. In Fig. 3, a solid black square ■ symbolizes a silicon oxide layer polished using a planar polishing pad (abrasive units); a empty square □ symbolizes a silicon oxide layer polished using a roughened polishing pad (abrasive units); a solid circle ● symbolizes a silicon nitride layer polished using a planar polishing pad (abrasive units); and, an empty circle O symbolizes a silicon nitride layer polished using a roughened polishing pad (abrasive units). As shown in Fig. 3, the removal rate for silicon nitride is low no matter if the surface of the polishing pad is smooth or rough. Hence, the method of this invention is particularly suitable for carrying out a chemical-mechanical polishing of a silicon oxide layer to form a shallow trench isolation (STI) structure. Furthermore, using a polishing pad with roughened surface has significantly higher removal rate than using a polishing pad with a smooth surface. Consequently, even if the silicon oxide layer on the surface of a wafer has already been planarized, deploying a polishing pad with a roughened surface still increases the polishing rate and provides a means of removing the silicon oxide layer.

[0033] Figs. 4A and 4B are schematic cross-sectional views showing the steps in an alternative method of polishing a wafer. As shown in Fig. 4A, a polishing station 400 is provided. The polishing station 400 has a wafer holder 202, a polishing pad 202 and a polishing platform 206 similar to the polishing stations 200 and 300 in the aforementioned embodiments. The wafer holder 202 has a retainer ring 203. The surface of the retainer ring 203 has a series of grooves 203a patterned in various forms including, for example, crosses (as shown in Fig. 5A), concentric circles (as shown in Fig. 5B), spirals (as shown in Fig. 5C) or any combination of the aforementioned shapes.

Furthermore, the groove pattern 203a is able to contact the polishing pad 302 when the wafer is polished.

[0034] The polishing pad 304 comprises a plurality of abrasive units 311. The abrasive units 311 are shaped into a triangular cone, hexagonal cone or circular cylinder and set up as an array. Each abrasive unit 311 comprises a layer of adhesive compound 210 with a plurality of evenly distributed abrasive particles 208 therein. The adhesive compound 210 is an adhesive resin, for example. Aside from the abrasive units 311, the polishing pad 302 also has a polishing platen (not shown) underneath. The platen is fabricated from a material including, aluminum alloy or stainless steel. Note that if the layer to be polished is a silicon oxide, cerium oxide (CeO_2) abrasive particles 208 are preferably used because it has a higher polishing selectivity relative to the silicon oxide.

[0035] As shown in Fig. 4A, the wafer holder 202 grips a silicon wafer 214 and presses onto the polishing pad 302 to carry out a first polishing operation so that the silicon oxide layer 212 on the wafer 214 is planarized. As the polishing operation is continued, the surface of the silicon oxide layer 212 is gradually flattened and hence the capacity to wipe away the adhesive compound 210 to expose the abrasive particles 208 is lost. However, the retainer ring 203 on the wafer holder 202 has groove patterns 203a in contact with the abrasive units 311 so that the surface of the abrasive units 311 is scraped and roughened up again.

[0036] As shown in Fig. 4B, the polishing operation is continued. In the presence of groove patterns on the retainer ring 203, the surface of the abrasive unit 311 is roughened in-situ. Since the retainer ring can roughen the surface of the polishing pad in-situ, the polishing rate will not drop as the surface of a polished layer (for

example, the silicon oxide layer 212) is gradually ground down. In other words, a constant polishing rate can be maintained when the surface of a structure is planarized.

[0037] Fig. 6 is a graph showing the effects various types of retainer ring grooves have on silicon oxide/silicon nitride polishing rate. In Fig. 6, a solid black square ■ symbolizes a silicon oxide layer polished using a wafer holder having a planar retainer ring surface; a empty square □ symbolizes a silicon oxide layer polished using a wafer holder having a roughened retainer ring surface; a solid circle ● symbolizes a silicon nitride layer polished using a wafer holder having a planar retainer ring surface; and, an empty circle O symbolizes a silicon nitride layer polished using a wafer holder having a roughened retainer ring surface. As shown in Fig. 6, the removal rate for a silicon nitride layer is low no matter if the surface of the polishing pad is smooth or rough. Hence, the method of this invention is particularly suitable for carrying out a chemical-mechanical polishing of a silicon oxide layer to form a shallow trench isolation (STI) structure. Furthermore, using a retainer ring with a groove pattern thereon has a significantly higher removal rate than using a retainer ring with a smooth surface. Consequently, even if the silicon oxide layer on the surface of a wafer has already been planarized, deploying a wafer holder with a roughened retainer ring surface still increases the polishing rate and provides a means of removing the silicon oxide layer.

[0038] This invention utilizes the roughened surface of a polishing pad (the polishing units) to perform a fixed abrasive chemical-mechanical polishing of a wafer. This resolves the issue of having a decreasing polishing efficiency due to a gradual lowering of the roughness of a polish surface. Hence, the time for completing a global

planarization is reduced and the possibility of having residual material on the polish surface is minimized.

[0039] Furthermore, because this invention uses the roughened surface of a polishing pad (the polishing units) to carry out a fixed abrasive chemical-mechanical polishing operation, thickness of the polishing layer no longer constitutes a restriction. This invention also removes the width restriction in a shallow trench isolation (STI) gap-fill process.

[0040] In addition, this invention also utilizes a wafer holder with a retainer ring having a groove pattern to execute a fixed abrasive chemical-mechanical wafer polishing operation. Through the groove pattern on the retainer ring, the polishing pad (the polishing units) is re-conditioned in-situ to maintain a rough surface. Therefore, the upper surface of the polishing pad is able to maintain a roughened surface despite the gradual reduction in the roughness level of the polished wafer.

[0041] If cerium oxide (CeO_2) is used as the abrasive particles in this invention, an optimal polishing selectivity between silicon oxide and silicon nitride is produced. Consequently, residual silicon oxide on a silicon nitride layer can be removed.

[0042] Finally, the polishing pad in this invention is fabricated using a plurality of abrasive units each comprising some adhesive compound enclosing a plurality of abrasive particles. However, the polishing pad may be fabricated as a single adhesive compound layer that encloses a plurality of evenly distributed abrasive particles.

[0043] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that

the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.